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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Mansoori et al.

Art Unit:

2812

Serial No.:

10/620,492

Examiner:

Lindsay, Jr., W.

Filing Date:

07/16/2003

Docket No.:

TI-35375

Customer No.: 23494

TI-35375 FAXED: 5/31/2005 DUE: 3/1/2005 ATTY/SEC'Y: JJG

22404

Conf. No.:

9069

Title: METHOD TO REDUCE TRANSISTOR GATE TO SOURCE/DRAIN OVERLAP

CAPACITANCE BY INCORPORATION OF CARBON

CERTIFICATION OF FACSIMILE TRANSMISSION

i hereby certify that the following papers are being transmitted by facsimile to the U.S. Patent and Trademark Office at 703-872-9306 on the date shown below:

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May 31, 2005

Date

FACSIMILE COVER SHEET

X FACSIMILE COVER SHEET NEW APPLICATION DECLARATION (# Pages) ASSIGNMENT (# Pages) FORMAL DRAWINGS X INFORMAL DRAWINGS (2 replacement sheets) CONTINUATION APP'N (# Pages) DIVISIONAL APP'N		X AMENDMENT (10 Pages) X EOT 3mth (2 Pages) NOTICE OF APPEAL (# Pages) APPEAL (# Pages) ISSUE FEE (# Pages) REPLY BRIEF (IN TRIPLICATE) (# Pages)				
NAME OF INVENTOR(S):		RECEI	PT DATE & SER	IAL NO.:		
Mansoori		Ser	ial No.:	10/620,492		
TITLE OF INVENTION:		Fili	ng Date:	07/16/2003	_	
Method to Reduce Transistor			nf. No.: 9		01PE/	NNL
TI FILE NO.:	DEPOSIT ACCT. NO.:	1				1
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